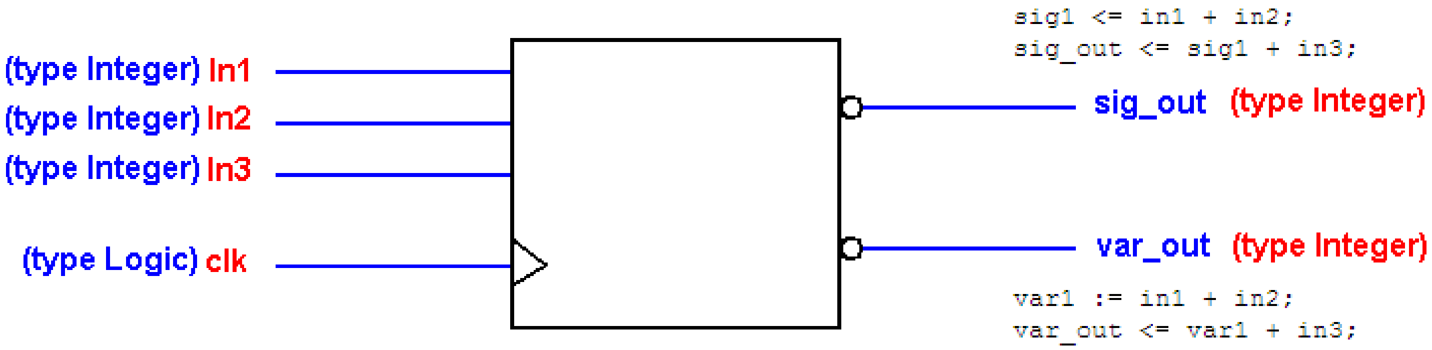
Signal and Variable

Some of the predefined types in VHDL:

Bit	'0' or '1'
Boolean	True or False
Integer	an integer in the range $-(2^{31} - 1)$ to $+(2^{31} - 1)$
Real	floating point number in the range -1.0E38 to +1.0E38
Character	any legal VHDL character including upper or lower case letter, digits, and special characters must be enclosed in single quotes, e.g. 'd', '7' or '+'.
Time	an integer with units fs, ps, ns, us, ms, sec, min, or hr etc.

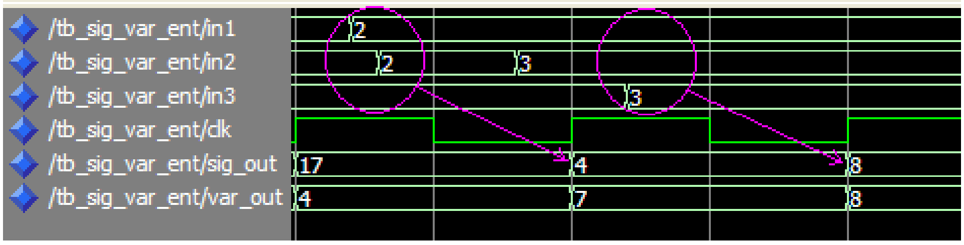
1. Signals are used to connect the design components and must carry the information between current statements of the design. On the other hand, variables are used within process to compute certain values.Variables must be declared inside a process

2. A variable changes instantaneously when the variable assignment is executed. On the other hand, a signal changes a delay after the assignment expression is evaluated. If no delay is specified, the signal will change after a delta delay. This has important consequences for the updated values of variables and signals.



```
sig1 <= in1 + in2;
sig_out <= sig1 + in3;
```

```
var1 := in1 + in2;
var_out <= var1 + in3;
```



VHDL CODE

```
===========================================================================
Sig_Var.vhdl
===========================================================================
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

--Hendra Kesuma
```

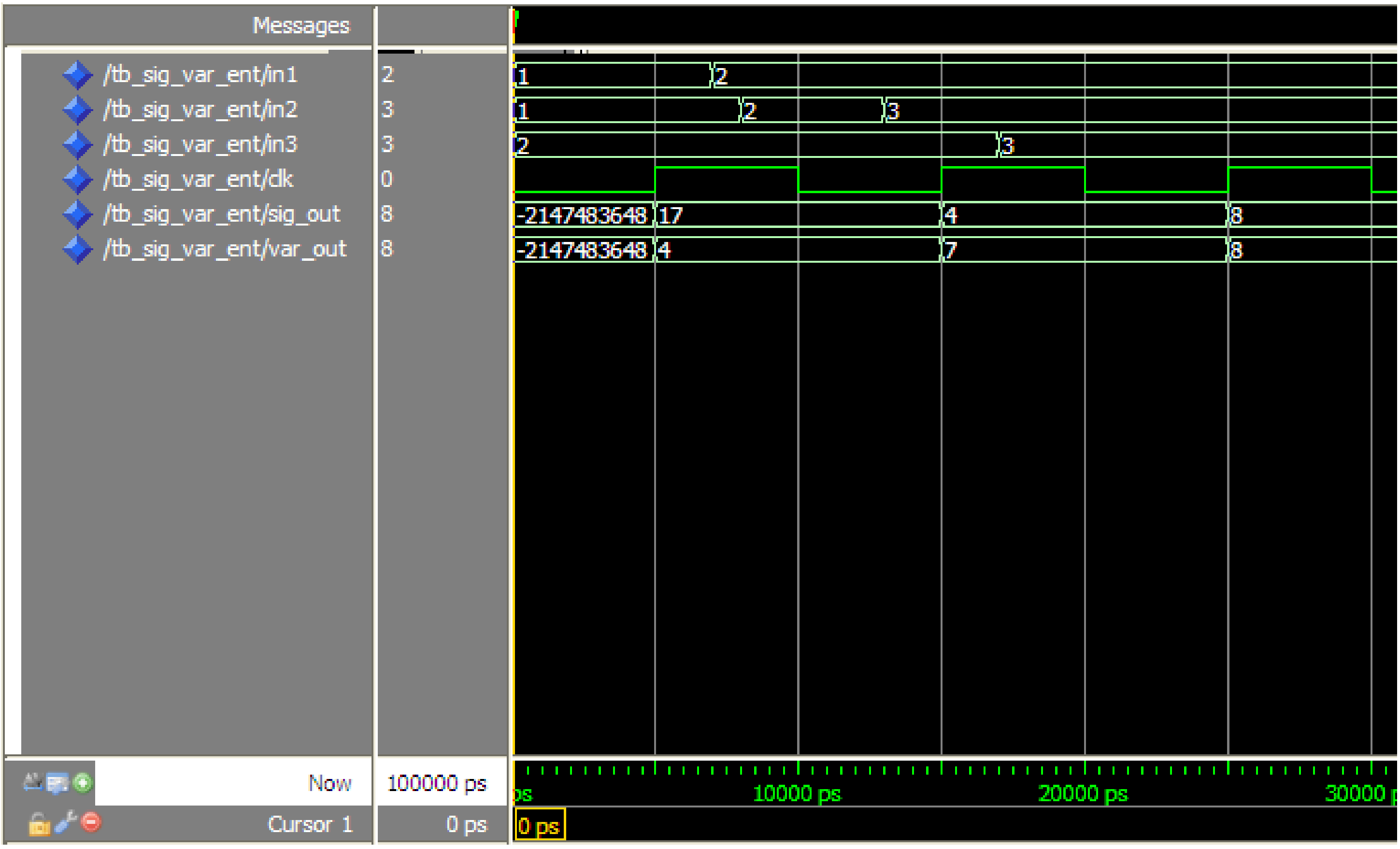
```
entity sig_var_ent is
    Port ( in1 : in  Integer;
           in2 : in  Integer;
           in3 : in  Integer;
           clk : in  STD_LOGIC;
           sig_out : out  Integer;
           var_out : out  Integer);
end sig_var_ent;

architecture sig_var_arch of sig_var_ent is
  signal sig1 : integer := 15;
begin
  p1:process(in1, in2, in3, clk)
    variable var1 : integer := 11;
   begin
            if clk = '1' and clk'event then
             var1 := in1 + in2;
             var_out <= var1 + in3;
    end if;
  end process;

  p2:process(in1, in2, in3, clk)
   begin
            if clk = '1' and clk'event then
             sig1 <= in1 + in2;
             sig_out <= sig1 + in3;
    end if;
  end process;

end sig_var_arch;
```

TESTBENCH CODE

```
==============================================================================
tb_sig_var_ent.vhd
==============================================================================
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

--Hendra Kesuma

ENTITY tb_sig_var_ent IS
END tb_sig_var_ent;

ARCHITECTURE tb_sig_var_arch OF tb_sig_var_ent IS

           -- Component Declaration for the Unit Under Test (UUT)
           COMPONENT sig_var_ent
           PORT(
               in1 : IN Integer;
               in2 : IN Integer;
               in3 : IN Integer;
               clk : IN std_logic;
               sig_out : OUT Integer;
               var_out : OUT Integer
               );
           END COMPONENT;

           --Inputs
           SIGNAL in1 :  Integer := 0;
           SIGNAL in2 :  Integer := 0;
           SIGNAL in3 :  Integer := 0;
           SIGNAL clk :  std_logic := '0';

           --Outputs
           SIGNAL sig_out :  Integer;
           SIGNAL var_out :  Integer;

BEGIN

           -- Instantiate the Unit Under Test (UUT)
           uut: sig_var_ent PORT MAP(
               in1 => in1,
               in2 => in2,
               in3 => in3,
               clk => clk,
               sig_out => sig_out,
               var_out => var_out
           );

           tb : PROCESS
           BEGIN

               -- Wait 100 ns for global reset to finish
               --wait for 100 ns;

               -- Place stimulus here
               in1<= 1 after 0 ns, 2 after 7 ns;
               in2<= 1 after 0 ns, 2 after 8 ns, 3 after 13 ns;
               in3<= 2 after 0 ns, 3 after 17 ns;

            loop
            clk <= '0';
            wait for 5 ns;
            clk <= '1';
            wait for 5 ns;
            end loop;

            wait; -- will wait forever
```

```
        END PROCESS;
END;
```

SIMULATION



```
Messages
/tb_sig_var_ent/in1       2
/tb_sig_var_ent/in2       3
/tb_sig_var_ent/in3       3
/tb_sig_var_ent/clk       0
/tb_sig_var_ent/sig_out   8
/tb_sig_var_ent/var_out   8
Now                       100000 ps
Cursor 1                  0 ps
```