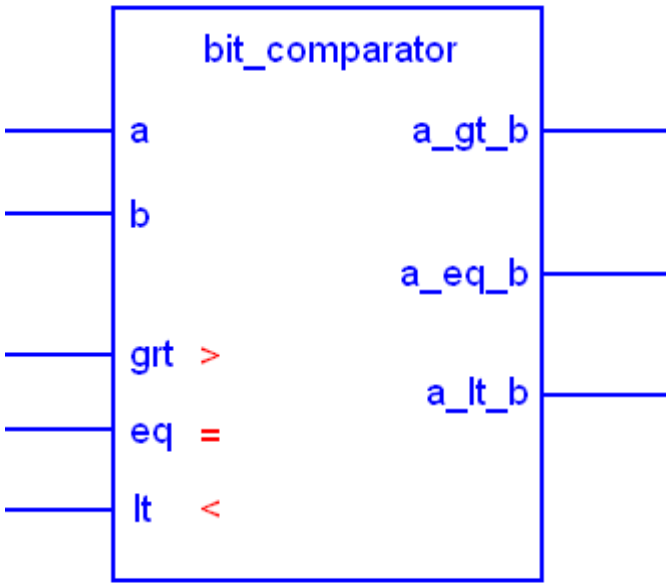
Functions and Procedures

In any high level language, subprogramms are used to simplify coding, modularity and reliability or description. VHDL also allows two forms of subprogramms, ***functions*** and ***procedures***. Function return value and cannot alter the values of their parameters.



single bit comparator

VHDL CODE

```
================================================================================
bit_comparator.vhdl
================================================================================
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Hendra Kesuma

entity ent_bit_comparator is
    Port ( a : in std_logic;
           b : in std_logic;
           grt : in std_logic;
           eq : in std_logic;
           lt : in std_logic;
           a_gt_b : out std_logic;
           a_eq_b : out std_logic;
           a_lt_b : out std_logic);
end ent_bit_comparator;
```

```
architecture arch_bit_comparator of ent_bit_comparator is

-- Function 1
      FUNCTION fgl(x, y, gl: std_logic) RETURN std_logic IS
        BEGIN
        RETURN ((x and  gl) or ((not y) and gl) or (x and (not y)));
      END fgl;

-- Function 2
     FUNCTION feq(x, y, equ: std_logic) RETURN std_logic IS
       BEGIN
       RETURN ((x and y and equ) or ((not x) and (not y) and equ));
     END feq;

  begin
     a_gt_b <= fgl(a, b, grt);
     a_eq_b <= feq(a, b, eq);
     a_lt_b <= fgl(b, a, lt);

end arch_bit_comparator;
```

TESTBENCH CODE

==========

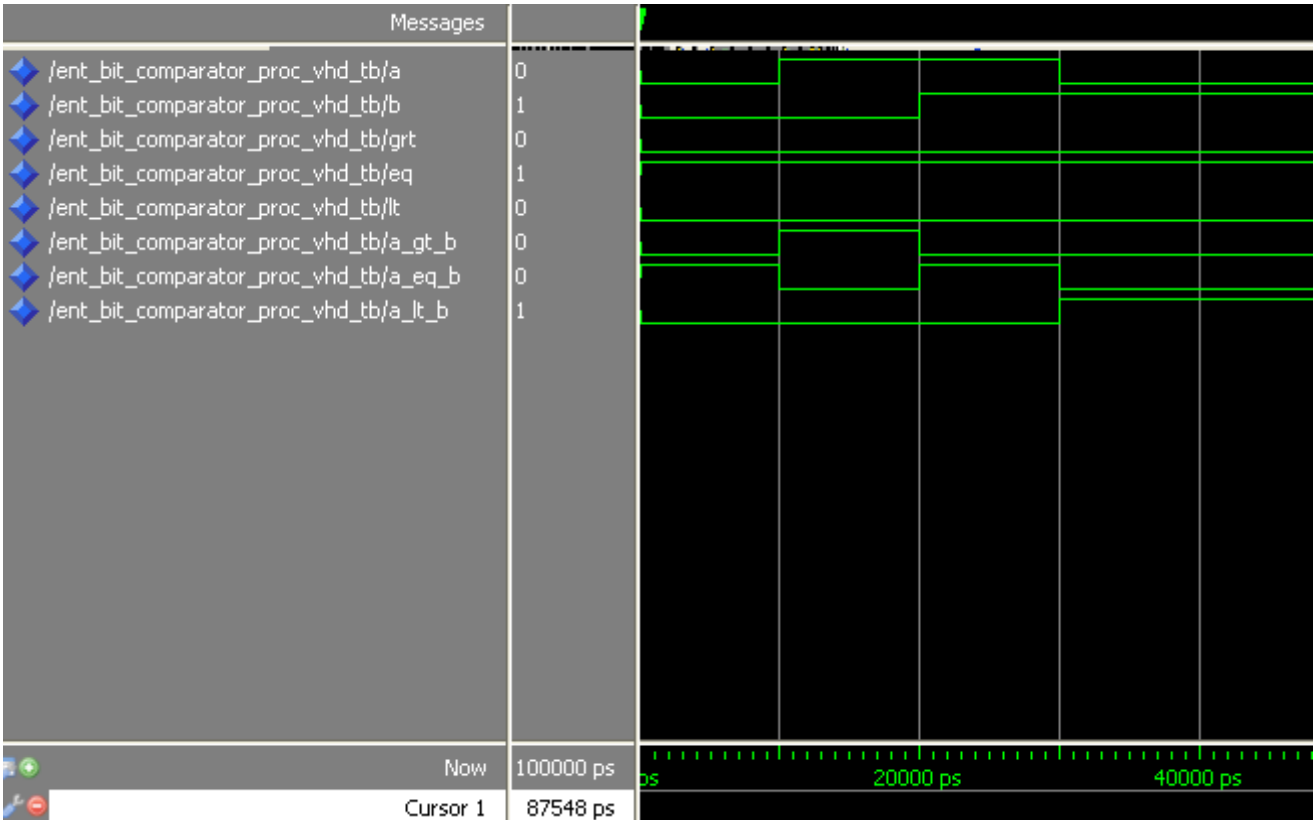
tb_bit_comparator.vhd

==========

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

-- Hendra Kesuma

ENTITY ent_bit_comparator_tb_bit_comparator_vhd_tb IS
END ent_bit_comparator_tb_bit_comparator_vhd_tb;

ARCHITECTURE behavior OF ent_bit_comparator_tb_bit_comparator_vhd_tb IS

        COMPONENT ent_bit_comparator
        PORT(
                a : IN std_logic;
                b : IN std_logic;
                grt : IN std_logic;
                eq : IN std_logic;
                lt : IN std_logic;
                a_gt_b : OUT std_logic;
                a_eq_b : OUT std_logic;
                a_lt_b : OUT std_logic
                );
        END COMPONENT;
```

```
        SIGNAL a :  std_logic;
        SIGNAL b :  std_logic;
        SIGNAL grt :  std_logic;
        SIGNAL eq :  std_logic;
        SIGNAL lt :  std_logic;
        SIGNAL a_gt_b :  std_logic;
        SIGNAL a_eq_b :  std_logic;
        SIGNAL a_lt_b :  std_logic;

BEGIN

        uut: ent_bit_comparator PORT MAP(
                a => a,
                b => b,
                grt => grt,
                eq => eq,
                lt => lt,
                a_gt_b => a_gt_b,
                a_eq_b => a_eq_b,
                a_lt_b => a_lt_b
        );


-- *** Test Bench - User Defined Section ***
        tb : PROCESS
             BEGIN

         a <= '0' after 0 ns,
              '1' after 10 ns,
              '0' after 30 ns;

         b <= '0' after 0 ns,
              '1' after 20 ns;

        grt <= '0' after 0 ns;

        eq <= '1' after 0 ns;

         lt <= '0' after 0 ns;

     wait; -- will wait forever
  END PROCESS;
-- *** End Test Bench - User Defined Section ***
```

SIMULATION



TESTBENCH CODE WITH PROCEDURE

```
================================================================================
tb_procedure_comparator.vhd
================================================================================
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

-- Hendra Kesuma

ENTITY ent_bit_comparator_Proc_vhd_tb IS
END ent_bit_comparator_Proc_vhd_tb;

ARCHITECTURE behavior OF ent_bit_comparator_Proc_vhd_tb IS

  PROCEDURE ApplyData_Procedure
        (signal   OutBit:                out  std_logic;
                  constant GivenBit:     in   std_logic_vector (0 to 3);
                  constant GivenPeriod : in   time) IS
  BEGIN
  OutBit <= transport GivenBit(0) after 0*GivenPeriod;
  OutBit <= transport GivenBit(1) after 1*GivenPeriod;
  OutBit <= transport GivenBit(2) after 2*GivenPeriod;
  OutBit <= transport GivenBit(3) after 3*GivenPeriod;
```

```
-------Or----------
--   for i in 0 to 3
--        OutBit <= transport GivenBit(i) after i*GivenPeriod;
--   end loop;

   END PROCEDURE ApplyData_Procedure;

        COMPONENT ent_bit_comparator
        PORT(
                a : IN std_logic;
                b : IN std_logic;
                grt : IN std_logic;
                eq : IN std_logic;
                lt : IN std_logic;
                a_gt_b : OUT std_logic;
                a_eq_b : OUT std_logic;
                a_lt_b : OUT std_logic
                );
        END COMPONENT;

        SIGNAL a :  std_logic;
        SIGNAL b :  std_logic;
        SIGNAL grt :  std_logic;
        SIGNAL eq :  std_logic;
        SIGNAL lt :  std_logic;
        SIGNAL a_gt_b :  std_logic;
        SIGNAL a_eq_b :  std_logic;
        SIGNAL a_lt_b :  std_logic;

BEGIN

        uut: ent_bit_comparator PORT MAP(
                a => a,
                b => b,
                grt => grt,
                eq => eq,
                lt => lt,
                a_gt_b => a_gt_b,
                a_eq_b => a_eq_b,
                a_lt_b => a_lt_b
        );

-- *** Test Bench - User Defined Section ***
   tb : PROCESS
        BEGIN
           grt <= '0' after 0 ns;
          eq  <= '1' after 0 ns;
           lt  <= '0' after 0 ns;
```

```
  ApplyData_Procedure(a, "0110", 10 ns);
  ApplyData_Procedure(b, "0011", 10 ns);

    wait; -- will wait forever
  END PROCESS;
-- *** End Test Bench - User Defined Section ***

END;
```